REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on February 26, 2003, and the references cited therewith.

Claim 42 is amended, no claims are canceled, and no claims are added; as a result, claims 1-42 are now pending in this application.

Information Disclosure Statement

Applicant respectfully requests that a copy of the 1449 Form, listing all references that were submitted with the Information Disclosure Statements filed on February 18, 2000 and November 13, 2000, marked as being considered and initialed by the Examiner, be returned with the next official communication.

Rejections Under 35 U.S.C. §103

The Office Action rejected claims 1-4, 6-8, 10-15, 21-31, and 37-41 as being unpatentable over Ishibashi et al. (US Patent No. 5, 621, 774; hereinafter referred to as Ishibashi) in view of Taya et al. (US Patent No. 5, 778, 214; hereinafter referred to as Taya), Konno (US Patent No. 5, 537,068; hereinafter referred to as Konno), and/or Gervasi (US Patent No. 5, 948, 083; hereinafter referred to as Gervasi).

The Examiner has the burden under 35 U.S.C. §103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To do that the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id.*

The *Fine* court stated that:

> Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221 USPQ at 933. And "teachings of references can be combined *only* if there is some suggestion or incentive to do so." *Id.* (emphasis in original).

The M.P.E.P. adopts this line of reasoning, stating that

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).

An invention can be obvious even though the suggestion to combine prior art teachings is not found in a specific reference. *In re Oetiker*, 24 USPQ2d 1443 (Fed. Cir. 1992). At the same time, however, although it is not necessary that the cited references or prior art specifically suggest making the combination, there must be some teaching somewhere which provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem which the claimed invention addresses. One of ordinary skill in the art will be presumed to know of any such teaching. (See, e.g., *In re Nilssen*, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988) and *In re Wood*, 599 F.2d 1032, 1037, 202 USPQ 171, 174 (CCPA 1979)).

Applicant respectfully submits that the Office Action does not make out a *prima facie* case of obviousness for the following two reasons: (1) even if combined, the cited references fail to teach or suggest all of the elements of applicant's claimed invention; and (2) there is no suggestion to combine the cited references because a suggestion to combine must come from the prior art and not from Applicant's specification or impermissible hindsight.

Regarding independent claim 1, the Office Action asserts that the combination of Ishibashi and Taya teaches all the elements of claim 1. In the following discussion, the teachings of Ishibashi and Taya will first be summarized and then the independent claim 1 will be analyzed with respect to the teachings of the references.

Ishibashi teaches a system for synchronizing parallel data transfer. The system includes an array of variable delay circuits (see Figure 8, reference numerals VD(0) - VD(n)), an array of latches (see Figure 8, reference numerals Lin(0) - Lin (n)), and a variable delay control circuit (see Figure 8, reference numeral 81). According to Ishibashi, the variable delay circuits (VD(0) – VD(n)) receive data signals (DT(0) – DT(n)). After a delay, the variable delay circuits forward

the data signals to the latches (Lin (0) to Lin (n)). The latches forward the data signals to the variable control circuit (81) based on a clock signal (CK).

Taya teaches compensating for skew in a delayed data signal by inserting a synchronizing pattern into the data signal. The data signal is then periodically sampled to determine whether each sample contains the synchronizing pattern. If the sample contains the synchronizing pattern, the data signal phase is proper. Otherwise, the data signal phase is corrected by adjusting the data signal delay.

Independent claim 1 recites "phase comparing each of the plurality of delayed signals to a reference signal to detect changes in the detected skew." The Office Action correctly points out that Taya's "bit-phase adjusting circuit 1 adjusts a phase difference between data signals and a clock by adjusting a delay of the data signal." The Office Action at page 3, quoting Taya at column 4, lines 37-39. However, the Office Action incorrectly asserts that Taya's bit-phase adjusting is the same as claim 1's "phase comparing." In contrast to claim 1, as summarized above, Taya checks for skew in a data signal by inserting a synchronization pattern into the data signal and later sampling the data signal. Taya's sampling and pattern matching is different from claim 1's comparing delayed signals to a reference signal. Therefore, neither Taya nor Ishibashi, alone or in combination, teach or suggest all the elements of independent claim 1.

In addition to not teaching all the claim elements, there is no suggestion to combine the cited references. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. The Examiner must avoid hindsight. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). The Office Action does not cite a passage from Ishibashi or Taya that teaches or suggests combining the teachings of the references. Without such a citation, Applicant respectfully submits that the Office Action impermissibly relied on the Applicant's disclosure and/or impermissible hindsight in forming the rejections under 35 USC §103 over the cited references.

Regarding independent claims 11, 27, and 39, the Office Action asserts that the combination of Ishibashi and Konno teaches all the elements of each of independent claims 11,

27, and 39. In particular, the Office Action asserts that the passage from Ishibashi at column 7, lines 36-47 teaches the rejected claims' first delay line and skew detection circuits. In particular, the Office Action asserts that Ishibashi's latches are the same as the skew detection circuits of independent claims 11, 27, and 39. The Office Action also asserts that Ishibashi's variable delay control circuit is the same as the claimed delay line controller.

As described in the summary above, Ishibashi teaches a system including an array of variable delay circuits for receiving a data signal. Ishibashi's system also teaches an array of latches (see Figure 8) for receiving a data signal from the variable delay circuits and transmitting the data signal to a variable delay control circuit based on a clock signal. In contrast to Ishibashi, the skew detection circuits of independent claims 11, 27, and 39 are not latches. The Free Online Dictionary Of Computing, defines a latch as:

> A digital logic circuit used to store one or more bits. A latch has a data input, a clock input and an output. When the clock input is active, data on the input is "latched" or stored and transferred to the output either immediately or when the clock input goes inactive. The output will then retain its value until the clock goes active again.

Therefore, a latch receives a data input and then transmits that data input. The skew detection circuits of claims 11, 27, and 39 are not latches for two reasons. First, the skew detection circuits include logic for comparing the phase of a data signal to the phase of a clock signal. Second, although each skew detection circuit receives a data signal, each skew detection circuit does not transmit that data signal. After receiving a data signal, each skew detection circuit transmits a data early or clock early signal (*not the data signal*) based on the phase comparison described above. Therefore, Ishibashi's latches are different from the skew detection circuits recited in claims 11, 27, and 39.

Additionally, Applicant respectfully submits that the Office Action has mischaracterized Ishibashi's variable delay control circuit as being the same as the claimed delay line controller. According to Ishibashi, the variable delay control circuit receives input from an array of latches (see above). However, in contrast, the claimed delay line control circuit does not receive input from an array of latches. The delay line control circuit receives input from the skew detection

circuit, which is not a latch (see above). Therefore, Ishibashi's variable delay control circuit does not teach the claimed delay line controller.

The only way for the combination of Ishibashi and Konno to teach or suggest all the elements of independent claims 11, 27, and 39 is for Konno to provide what Ishibashi is lacking. Konno teaches a differential delay line clock generator, but does not teach or suggest a skew detection circuit, as recited in claims 11, 27, and 39. The Office Action does not point to a passage in Konno that teaches skew detection circuits, and Applicant knows of no such passage. Therefore, the combination of Ishibashi and Konno does not teach or suggest every element of independent claims 11, 27, and 39.

In addition to not teaching all the claim elements, there is no suggestion to combine the cited references. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. The Examiner must avoid hindsight. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). The Office Action does not cite a passage from Ishibashi or Konno that teaches or suggests combining the teachings of the references. Without such a citation, Applicant respectfully submits that the Office Action impermissibly relied on the Applicant's disclosure and/or impermissible hindsight in forming the rejections under 35 USC §103 over the cited references.

Regarding independent claim 25, the Office Action asserts that the combination of Ishibashi and Konno teaches all the elements of independent claim 25. The Office Action asserts that Ishabashi's latch circuit outputs are equivalent to the claimed skew indicator inputs. In particular the Office Action states:

> The outputs of latch circuits $L_{in}(0)$ to $L_{in}(n)$ is [sic] equivalent to claimed plurality of skew indicator signal inputs, wherein each skew indicator signal input is capable of receiving a skew indicator signal reflecting skew between one of the delayed input signals and a reference signal in claim 25, lines 4-6.

Applicant respectfully submits that the skew indicator signal inputs are different from Ishibashi's latch outputs. According to Ishibashi, the latch outputs $L_{in}(0)$ to $L_{in}(n)$ merely transmit data signals DT(0) – DT(1), which were received from upstream, to a variable delay

controller circuit (see summary above). In contrast, the skew indicator signal inputs do not transmit data signals received from upstream. The skew indicator signal inputs transmit a "data early" signal or a "clock early" signal based on whether a data signal is in phase with a reference signal (e.g., a reference clock signal). Therefore, Ishibashi's latch outputs are different from the claimed skew indicator outputs.

The Office Action also asserts that Konno teaches a "means for gradually applying a control signal." The Office Action goes on to quote the following passage from Konno: "Low-pass filter (LPF22) smoothes the output of CP 21 before applying the control signal to VCO 23" Konno at column 2, lines 5-7.

Applicant respectfully submits that Konno does not teach or suggest any element of independent claim 25 for the following reasons. Firstly, the "means" cited by the Office Action is not an element in independent claim 25. Therefore, even if Konno taught such a "means," the means would not teach or suggest any element of independent claim 25. Secondly, regardless of any assertion made in the Office Action, Konno's low-pass filter is different than the claimed digital filter. In particular Konno teaches a low-pass filter for smoothing the output of a charge pump (see Konno's Figure 3). Konno teaches a phase-locked-loop including a charge pump, a phase-frequency detector, and a low-pass filter. According to Konno, the use of a phase-frequency detector and charge-pump in the phase-locked-loop eliminates skew between two clock signals. Thus, delays between the clock signals are eliminated before they are transmitted to the low-pass filter. Because the low-pass filter receives clock signals that are in-phase, the low-pass filter does not generate "a delay control signal associated with one of the delayed input signals," as recited in independent claim 25. Based on the foregoing, Applicant respectfully submits that the combination of Ishibashi and Kommo does not teach or suggest all the elements of independent claim 25.

Regarding independent claim 40, the Office Action asserts that the combination of Ishibashi and Gervasi teaches all the elements of independent claim 40. In rejecting independent claim 40, the Office Action asserts that Ishabashi's latch circuits are equivalent to the claimed phase comparators. However, the Office Action has mischaracterized Ishabashi's latch circuits. As described above, a latch receives an input signal, stores the input signal, and transmits the

input signal. Similarly, Ishibashi's latch circuits receive a data signal and transmits that data signal to a variable delay control circuit. Ishibashi's latch circuits do not perform the operations of a comparator. Therefore, Ishibashi does not teach or suggest providing a phase comparator, as recited in independent claim 40.

Claim 40 also recites "driving the phase comparator with a clock having 2 edges per data bit and a 50% duty cycle, wherein driving includes sensing the clock and determining an error signal indicating drift from the 50% duty cycle." The Office Action admits that Ishibashi does not teach this element of independent claim 40. The Office Action goes on to assert that Gervasi teaches an alternate method of latching. However, in describing Gervasi, the Office Action does not point to a passage in Gervasi that teaches the claimed "driving," and Applicant knows of no such passage. Therefore, the combination of Ishibashi and Gervasi do not teach or suggest all the elements of claim 40.

In addition to not teaching all the claim elements, there is no suggestion to combine the cited references. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. The Examiner must avoid hindsight. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). The Office Action does not cite a passage from Ishibashi or Gervasi that teaches or suggests combining the teachings of the references. Without such a citation, Applicant respectfully submits that the Office Action impermissibly relied on the Applicant's disclosure and/or impermissible hindsight in forming the rejections under 35 USC §103 over the cited references.

Claims 2-4, 6-8, 10, 12-15, 21-24, 26 and 28-31 and 37-38, and 41 depend, directly or indirectly, on claims 1, 11, 25, 27, 39, or 40, and are patentable over the cited references for the reasons argued above, plus the elements in the claims.

Rejections under 35 U.S.C. §112

The Office Action rejected claim 42 under 35 U.S.C. §112 as being indefinite. Claim 42 has been amended to define the acronym DMC as Data Minus Clock. Applicant respectfully

submits that the amendment overcomes this rejection and that the claim is in condition for allowance.

Allowable Subject Matter

Claims 5, 9, 16-20, and 32-36 were objected to as being dependent upon a rejected base claims 3, 7, 11, and 27, respectively, but was indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant thanks the Examiner for indicating this allowable subject matter. Applicant respectfully submits these claims are in condition for allowance because they depend from claims that are patentable over the cited references, as explained above.

Reservation of Rights

Applicant does not admit that references cited under 35 U.S.C. §§ 102(a), 102(e), 103/102(a), or 103/102(e) are prior art, and reserves the right to swear behind them at a later date. Arguments presented to distinguish such references should not be construed as admissions that the references are prior art.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 371-2169) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 27th day of May, 2003.

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Signature